CLAIMS

We claim:

1 A semiconductor device comprising:

a first dielectric layer formed on a substrate;

a second dielectric layer formed on the first dielectric layer;

a stud formed through the first and second dielectric layers;

a third dielectric layer formed over a top of the stud; and

a first pad of first etch stop material formed over the top surface of the stud and under the third dielectric layer.

2 The semiconductor device of claim 1 wherein the pad is formed in a void region remaining after removal of a portion of the second dielectric layer.

3 The semiconductor device of claim 1 further comprising:

a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and

a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material.

4 The semiconductor device of claim 1 wherein the third dielectric layer and the first etch stop material are the same material.

5 The semiconductor device of claim 1 further comprising a second pad of a second etch stop material formed over the top surface of the stud and the first pad of the first etch stop material, the second pad of the second etch stop material being selectively patterned to cover only an area of the semiconductor device that includes the stud.

6 The semiconductor device of claim 5 wherein the third dielectric layer, and the first and second etch stop materials are the same material.

7 The semiconductor device of claim 1 further comprising:

a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and

a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material, whereby the spacers and the first pad are formed simultaneously.

8 The semiconductor device of claim 1 wherein the third dielectric layer has an etch selectivity with respect to the second dielectric layer.

9 The semiconductor device of claim 1 wherein the third dielectric layer comprises etch stop material.

10 A method of forming a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a second dielectric layer on the first dielectric layer;

forming a stud through the first and second dielectric layers;

forming a third dielectric layer over the top of the stud and the second dielectric layer;

removing a portion of the second dielectric layer at the top of the stud, to create a void region in the second dielectric layer at the top of the stud and under the third dielectric layer; and

forming a first pad of a first etch stop material in the void region.

11 The method of claim 10 further comprising:

forming a first circuit region in the first dielectric layer, the first circuit region including the stud;

forming a second circuit region in the first dielectric layer, the second circuit region including at least one conductive line.

12 The method of claim 11 further comprising forming a spacer of the first etch stop material on a sidewall of the conductive line while the pad of the first etch stop material is formed in the void region.

13 The method of claim 10 wherein the third dielectric layer and the first etch stop materials are the same material.

14 The method of claim 10 further comprising forming a second pad of a second etch stop material over the top surface of the stud and the first pad of the first etch stop material.

15 The method of claim 14 wherein the third dielectric layer material and the first and second etch stop materials are the same material.

16 The method of claim 14 wherein forming the second pad of the second etch stop material comprises:

forming a layer of the second etch stop material on the device;

selectively removing the layer of the second etch stop material to leave the second pad of the second etch stop material over the stud.

17 The method of claim 10 wherein the step of removing removes a top portion of the stud to further expose the second dielectric layer at the top of the stud.